

### REMARKS

This Amendment responds to the Office Action dated July 27, 2004 in which the Examiner required a new title, objected to claim 5, rejected claims 1-11 under 35 U.S.C. §112, second paragraph and under 35 U.S.C. §102(e).

Applicants know of no Power of Attorney submitted on March 31, 2003.

As indicated above, a new title has been provided which clearly indicates the invention to which the claims are directed. Therefore, applicant therefore respectfully requests the Examiner approves the new title.

As indicated above, minor informalities in the specification have been corrected. Applicants respectfully request the Examiner approves the corrections.

As indicated above, claim 5 has been amended to correct an informality. Applicants respectfully request the Examiner approves the correction and withdraws the objection to claim 5.

As indicated above, claims 1-11 have been amended in order to more particularly point out and distinctly claim the subject matter which the applicant regards as the invention. Therefore, applicants respectfully request the Examiner withdraws the rejection to the claims under 35 U.S.C. §112, second paragraph.

As indicated above, claims 3, 5, 7, 11 have been rewritten into independent form.

Claims 1-11 were rejected under 35 U.S.C. §102(e) as being anticipated by *Sato* (U.S. Patent No. 6,345,357).

Applicant respectfully traverses the Examiner's rejection of claims under 35 U.S.C. §102(e). The claims have been reviewed in light of the Office Action, and for

reasons which will set forth below, Applicant respectfully requests the Examiner withdraws the rejection to the claims and allows the claims to issue.

*Sato* appears to disclose at column 13, line 65 through column 14, line 18, that instructions  $N + 8$  through  $N + 12$  are all fetched but are made NOP. Thus nothing in *Sato* shows, teaches or suggests switching the instruction processing sequence to a next instruction of a repeat block at an instruction fetch stage as claimed in claim 3. Applicant respectfully submits that as claimed in claim 3, the processing is switched such that (using Figure 12 of *Sato* as an example) the next fetched instruction is instruction  $N + 13$  when instruction  $N + 7$  is fetched and before the instruction  $N + 7$  is performed. Since no instructions from instruction  $N + 8$  to instruction  $N + 12$  are fetched in the present invention, they are therefore not performed and not fetched. However, *Sato* clearly discloses that instructions  $N + 8$  through  $N + 12$  are all fetched but not performed by NOP.

Additionally, *Sato* merely discloses at column 7, line 64 through column 8, line 9 returning to the first instruction in the repeat block during repeat processing. Thus, nothing in *Sato* shows, teaches or suggests performing jump processing to the next instruction of the repeat block during execution of the last instruction that is executed last in the repeat processing of the repeat block as claimed in claim 5. Rather, *Sato* merely discloses returning to the first instruction in the repeat block during repeat processing.

Furthermore, *Sato* merely discloses at column 10, lines 50-61, that the repeat end flag is determined based on the result of counting by SRPT-C register 188. In other words, the end of the repeat is determined by the number of instructions performed in the repeat processing of *Sato*. However, as claimed in claim 7,

deciding whether the repeat processing breaks is based upon an address of an instruction that is executed during the repeat processing of the repeat block in addition to the address of the last instruction in repeat processing. Thus, as claimed in claim 7, in order to determine the end of repeat processing, a break address is determined in addition to the address of the last instruction during repeat processing. In *Sato*, there is no disclosure about determining of repeat processing utilizing an address of instruction which is performed the latest during the repeat processing.

Finally, *Sato* merely discloses at column 15, line 62 through column 16, line 47 a hardware resource for step repeat maybe added to the hardware resource for a block repeat. Nothing in *Sato* shows, teaches or suggests determining a break based upon two different counters as claimed in claim 11. Rather, *Sato* merely discloses a hardware resource for step repeat may be added to the hardware resource for block repeat.

Since nothing in *Sato* shows, teaches or suggests the features as claimed in claims 3, 5, 7 and 11, as discussed above, Applicant respectfully requests the Examiner withdraws the rejection to claims 3, 5, 7 and 11 under 35 U.S.C. §102(e).

Claim 8 depends from claim 7 and recites additional features. Applicant respectfully submits that claim 8 would not have been anticipated by *Sato* within the meaning of 35 U.S.C. s102(e) at least for the reasons as set forth above. Therefore, Applicant respectfully requests the Examiner withdraws the rejection to claim 8 under 35 U.S.C. §102(e).

The prior art of record, which is not relied upon, is acknowledged. The references taken singularly or in combination do not anticipate or make obvious the claimed invention.

Thus it now appears that the application is in condition for reconsideration and allowance. Reconsideration and allowance at an early date are respectfully requested.

If for any reason the Examiner feels that the application is not now in condition for allowance, the Examiner is respectfully requested to contact, by telephone, the applicant's undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this case.


In the event that this paper is not timely filed within the currently set shortened statutory period, applicant respectfully petitions for an appropriate extension of time. The fees for such extension of time may be charged to our Deposit Account No. 02-4800.

In the event that any additional fees are due with this paper, please charge our Deposit Account No. 02-4800.

Respectfully submitted,

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